REMARKS

Claims 1-72 are pending in this application. Claims 1, 5, 9, 13, 19, 24, 27, 33, 38, 43, 49, 54, 59, 63 and 68 are independent claims.

Applicant has canceled claims 59-72 and added new claims 73-82. No new matter has been added.

Applicants have canceled the claims having features not shown in the drawings.

Applicants maintain that the current title is brief but technically accurate and descriptive and contains less than 500 characters. Accordingly, the title is proper under 37 CFR §1.72 (MPEP §606) and the examiner's objection to the title should be withdrawn.

The examiner rejected claims 59-72 under 35 USC §112, first paragraph, as failing to comply with the written description and enablement requirements.

Applicants have canceled claims 59-72.

The examiner uses Sidwell to reject claims 1, 5, 9 and 19 as having been anticipated.

Claim 1 recites "load a first portion of bits of a source into a first portion of a destination register and duplicate that first portion of bits in a subsequent portion of the destination register." Sidwell does not disclose or suggest this quoted claim feature. Sidwell does not duplicate a first portion of bits in a destination register to a subsequent portion of the same destination register. On the contrary, Sidwell does not manipulate the bits in the destination register in any fashion. Sidwell merely maniputes various portions of a source register in multiplexers for placement into a destination register. Once placed in the destination register, Sidwell is done. More specifically, Sidwell discloses:

> The byte replicate unit thus takes the least significant object (8, 16 or 32 bits) of the source operand and replicates it 8, 4, or 2 times, to produce the packed 64 bit result held in output buffer 112. (Page 6, paragraph 1)

This is quite different from applicants' claimed feature in which bits in the destination register are duplicated for placement into the same destination register. Accordingly, claim 1 is not anticipated by Sidwell.

Claims 5 and 9 recite "duplicating the first portion of bits in a subsequent portion of the destination register," or similar language. Claim 19 recites "loading a first number N of bits from a source into a lower half of a 2N wide-bit destination register and in a upper half of the 2N-bit wide destination register." Sidewell neither describes nor suggests these quoted features, as discussed with reference to claim 1 above. Accordingly, claims 5, 9 and 19 are not anticipated by Sidwell.

New independent claim 73 recites "load a first portion of bits of the source register into a first portion of the destination register and duplicate that first portion of bits in a subsequent portion of the destination register." New independent claim 77 recites "load 64-bits of the source register and return the 64-bits in a lower half of the destination register and a upper half of the destination register." For at least some the reasons stated above with respect to claim 1, new independent claims 73 and 77 are not anticipated by Sidwell.

The examiner uses Sidwell in combination with knowledge common to one of ordinary skilled in the art to reject claims 2-4, 6-8, 10-18 and 20-58.

Claim 13 recites "to load 64-bits of a source and return the 64-bits in a lower half of a destination and a upper half of a destination." At least this quoted claim feature is totally absent from Sidwell. Sidwell teaches combining bits from a source register with output from multiplexors to write an output into a destination register. This does not teach or suggest loading 64-bits of a source and returning the 64-bits in a lower half of a destination and an upper half of a destination. One would not be lead to Sidwell to provide this quoted feature because Sidwell provides no duplication whatsoever. Accordingly, claim 13 is not rendered obvious by Sidwell.

Claim 24 recites "load 64-bits from a source in a lower half of a 128-bit destination register and in an upper half of the 128-bit destination register." Claim 27 recites "load bits [127-0] of a source and return bits [63-32] of the source in bits [31-0] of a 128-bit destination register, bits [63-32] of the source in bits [63-32] of the destination register, bits [127-96] of the source in bits [95-64] of the destination register and bits [127-96] of the source in bits [127-96] of the destination register." Claim 33 recites "returning bits [63-32] of the source in bits [31-0] and bits [63-32] of the destination register and bits [127-96] of the source in bits [95-64] and bits [127-

96] of the destination register." Claim 38 recites "return bits [63-32] of the source in bits [31-0] of a 128-bit destination register, return bits [63-32] of the source in bits [63-32] of the destination register, return bits [127-96] of the source in bits [95-64] of the destination register, and return bits [127-96] of the source in bits [127-96] of the destination register." Claim 43 recites "load bits [127-0] of a source and return bits [31-0] of the source in bits [31-0] of a 128-bit destination register, bits [31-0] of the source in bits [63-32] of the destination register, bits [95-64] of the source in bits [95-64] of the destination register and bits [95-64] of the source in bits [127-96] of the destination register." Claim 49 recites "loading bits [127-0] of a source, returning bits [31-0] of the source in bits [31-0] of a 128-bit destination register, returning bits [31-0] of the source in bits [63-32] of the destination register, returning bits [95-64] of the source in bits [95-64] of the destination register and returning bits [95-64] of the source in bits [127-96] of the destination register." Claim 54 recites "return bits [31-0] of the source in bits [31-0] of a 128-bit destination register, return bits [31-0] of the source in bits [63-32] of the destination register, return bits [95-64] of the source in bits [95-64] of the destination register, and return bits [95-64] of the source in bits [127-96] of the destination register." For at least the reasons discussed with respect to claim 13 above, claims 24, 27, 33, 38, 43, 49 and 54 are not rendered obvious by Sidwell.

Independent claims 1, 5, 9, 13, 24, 27, 33, 38, 43, 49 and 54 are not rendered obvious by Sidwell. Claims 2-4, 6-8, 10-12, 14-18, 20-23, 25, 26, 28-32, 34-37, 39-42, 44-58, and 50-53 depend upon, and further limit, independent claims 1, 5, 9, 13, 24, 27, 33, 38, 43, 49 and 54. Accordingly, claims 2-4, 6-8, 10-12, 14-18, 20-23, 25, 26, 28-32, 34-37, 39-42, 44-58, and 50-53 are not rendered obvious by Sidwell.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this

paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

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